REMARKS/ARGUMENTS

Claims 1-13 were previously pending in the application. Claim 10 is amended; and new claims 14-24 are added herein. Assuming the entry of this amendment, claims 1-24 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Support for new claims 14-17 and 20-24 is found in Fig. 2, support for new claim 18 is found in original claim 12, and support for new claim 19 is found in original claim 13.

Objection to Drawings

On page 2 of the office action, the Examiner objected to the drawings under 37 CFR 1.83(a) for failing to show every feature of the invention specified in the claims. In particular, the Examiner stated that "the circuit that controls the switch devices ... must be shown (as recited in claims 6–8) or the feature(s) canceled from the claim(s)."

In response, the Applicant submits that the circuit described by the Examiner is not a "feature of the invention specified in the claims." For example, claim 6 recites that "the plurality of switch devices are individually controllable." This implies that each switch device can be opened or closed independent of the state of any other of the switch devices. This in turn implies that distinct control signals are used to control the states of the different switch devices. Significantly, there is no recitation in claim 6 as to the source of those control signals.

Claim 6, which depends from claim 5, which itself depends from claim 1, is directed to a programmable device, such as an FPGA (as recited, for example, in claim 8). Although the circuitry used to generate the control signals for the plurality of switch devices is usually implemented within the programmable device, there is nothing in the invention of claim 6 that requires such control circuitry to be implemented within the programmable device. This further supports the statement that a "controller" that controls the switch devices is not a specified feature of the invention of claim 6.

Similar arguments can be made in support of the statement that such a controller is not a specified feature of the invention of either claim 7 or claim 8.

In view of the foregoing, the Applicant submits that the objection to the drawings has been overcome.

Objection to the Disclosure

On page 3, the Examiner objected to the disclosure. In response, the Applicant has amended the disclosure as suggested by the Examiner.

Prior-Art Rejections

On page 3, the Examiner rejected claims 1-5, 9, and 11 under 35 U.S.C. 102(b) as being anticipated by McGowan. On page 6, the Examiner allowed claims 12-13 and objected to claims 6-8 and 10 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over McGowan.

Claim 1

Claim 1 is directed to a programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry. The programmable device comprises a first pad and a programmable I/O circuit (PIC) associated with the first pad. The PIC comprises (a) a first output buffer adapted to present a first outgoing signal at the first pad and (b) a first transmission gate connected between the first pad and the first output buffer. The first transmission gate is adapted to be closed when the first output buffer is selected to present the first outgoing signal at the first pad, and the first transmission gate is adapted to be open when the first output buffer is selected not to present the first outgoing signal at the first pad, wherein capacitive loading at the first pad due to the first output buffer is lower when the first transmission gate is open than when the first transmission gate is closed.

In rejecting claim 1, on page 3, the Examiner stated that McGowan discloses a first pad, a first output buffer, and a first transmission gate, citing, as examples, elements 30, 28-2, and 32-1 of Fig. 1, respectively. The Applicant submits that the Examiner mischaracterized the teachings in McGowan in rejecting claim 1.

In particular, while it is true that (i) element 30 is an example of a pad and (ii) element 32-1 is an example of a transmission gate that controls whether or not element 28-2 is operatively connected to pad 30, there is no teaching or even suggestion in McGowan that element 28-2 is an output buffer.

If anything, McGowan teaches away from element 28-2 being an output buffer. According to column 7, lines 22-25, analog circuit 28-2 "may be connected to I/O pads 30 through I/O buffers not shown." If analog circuit 28-2 were itself an output buffer, there would be little if any need to implement an I/O buffer between analog circuit 28-2 and its corresponding pad 30.

Moreover, there is no teaching or even suggestion in McGowan that capacitive loading at pad 30 due to analog circuit 28-2 is lower when pass gate 32-1 is open than when pass gate 32-1 is closed. The Examiner states that this feature is "inherent when the load is connected to pad 30." The Examiner appears to have confused an external load connected to pad 30 with the capacitive loading recited in claim 1. Claim 1 refers to the capacitive loading at the first pad "due to the first output buffer," not loading at the first pad due to some external load connected to the pad.

For all these reasons, the Applicant submits that McGowan does not teach or even suggest the combination of features recited in claim 1. As such, the Applicant submits that the rejection of claim 1 based on the mischaracterization of the teachings in McGowan is improper and that claim 1 is allowable over McGowan. Since claims 2-8 and 14-19 depend variously from claim 1, it is further submitted that those claims are also allowable over McGowan.

Claim 9

Claim 9 is directed to a programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry. The programmable device comprises a plurality of pads, a programmable I/O circuit (PIC) associated with the pads, and a transmission gate. The PIC comprises (a) a plurality of single-ended output buffers, each associated with at least one pad and (b) at least one double-ended output buffer associated with at least two pads. The transmission gate is connected between each single-ended output buffer and its at least one associated pad.

In rejecting claim 9, on page 5 of the office action, the Examiner stated that McGowan discloses "at least one double-ended output buffer," citing element 28-1 of Fig. 1 and column 7, lines 22+. The Applicant submits that the Examiner has mischaracterized the teachings in McGowan in rejecting claim 9.

In particular, McGowan defines element 28-1 of Fig. 1 as an analog circuit that is connected to two different pads 30. See column 7, lines 21-22, and Fig. 1. There is no teaching or even suggestion in McGowan that analog circuit 28-1 is "a double-ended output buffer." Rather, the only teaching in McGowan of a functional implementation for analog circuit 28-1 is as a comparator that compares two analog input signals V_{sense} and V_{ref} applied to two pads and generates a digital output signal that is applied to the internal FPGA portion 12 of the integrated circuit 10 of Fig. 1. See column 7, lines 44-49.

Thus, while it is true that Fig. 1 shows analog circuit 28-1 connected to two different pads, there is no teaching or even suggestion in McGowan that analog circuit 28-1 is a double-ended output buffer.

If anything, McGowan teaches away from analog circuit 28-1 being an output buffer at all. According to column 7, lines 22-25, analog circuit 28-1 "may be connected to I/O pads 30 through I/O buffers not shown." If analog circuit 28-1 were itself an output buffer, there would be little if any need to implement an I/O buffer between analog circuit 28-1 and its corresponding pads 30.

For all these reasons, the Applicant submits that McGowan does not teach or even suggest that analog circuit 28-1 is a double-ended output buffer. As such, the Applicant submits that the rejection of claim 9 based on the mischaracterization of the teachings in McGowan is improper and that claim 9 is allowable over McGowan. Since claims 10-11 and 20-23 depend variously from claim 1, it is further submitted that those claims are also allowable over McGowan.

Claim 14

According to new claim 14, the programmable device further comprises a second pad, and the PIC further comprises a second transmission gate connected between the first output buffer and the second pad. Thus, in the invention of new claim 14, the first output buffer is connected (a) to the first pad through the first transmission gate and (b) to the second pad through the second transmission gate.

McGowan does not teach or even suggest an output buffer connected to two different pads through two corresponding transmission gates. As such, the Applicant submits that this provides additional reasons for the allowability of claim 14 (and therefore claim 15) over McGowan.

Claim 15

According to new claim 15, the PIC further comprises one or more other output buffers, a first set of one or more other transmission gates, and a second set of one or more other transmission gates. Each transmission gate in the first set is connected between the first pad and a corresponding other output buffer, and each transmission gate in the second set is connected between the second pad and a corresponding other output buffer.

Fig. 2 shows an example of the invention of claim 15, which depends variously from claims 1 and 14. In this exemplary embodiment:

- Pad A is an example of the first pad of claim 1;
- Output buffer 202a is an example of the first output buffer of claim 1;

- o Transmission gate 214a is an example of the first transmission gate of claim 1;
- o Pad B is an example of the second pad of claim 14;
- o Transmission gate 216a is an example of the second transmission gate of claim 14;
- o Output buffers 202b, 202c are examples of the one or more other output buffers of claim 15;
- o Transmission gates 214b, 214c are examples of the first set of one or more other transmission gates of claim 15; and
- o Transmission gates 216b, 216c are examples of the second set of one or more other transmission gates of claim 15.

McGowan does not teach or even suggest such a combination of features. As such, the Applicant submits that this provides additional reasons for the allowability of claim 15 over McGowan.

Claim 16

According to new claim 16, the programmable device further comprises a second pad, and the PIC further comprises a double-ended output buffer associated with the first and second pads. Thus, in the invention of claim 16, the first output buffer and the double-ended output buffer are both associated with the first pad.

McGowan does not teach or even suggest two different output buffers associated with a single pad, where one of the output buffers is a double-ended output buffer. As such, the Applicant submits that this provides additional reasons for the allowability of claim 16 (and therefore claim 17) over McGowan.

Claim 17

According to new claim 17, the first output buffer is a single-ended output buffer, and the programmable device further comprises third and fourth pads. In addition, the PIC further comprises (a) a second transmission gate connected between the first single-ended output buffer and the third pad, (b) a first set of one or more other single-ended output buffers, (c) a second set of one or more other single-ended output buffers, (d) a first set of one or more transmission gates, each connected between the first pad and a corresponding single-ended output buffer of the first set, (e) a second set of one or more transmission gates, each connected between the second pad and a corresponding single-ended output buffer of the second set, (f) a third set of one or more transmission gates, each connected between the third pad and a corresponding single-ended output buffer of the first set, and (g) a fourth set of one or more transmission gates, each connected between the fourth pad and a corresponding single-ended output buffer of second first set.

Fig. 2 shows an example of the invention of claim 17, which depends variously from claims 1 and 16. In this exemplary embodiment:

- o Pad A is an example of the first pad of claim 1;
- o Output buffer 202a is an example of the first output buffer of claim 1;
- o Transmission gate 214a is an example of the first transmission gate of claim 1;
- o Pad C is an example of the second pad of claim 16;
- o Output buffer 212 is an example of the double-ended output buffer of claim 16;
- o Pad B is an example of the third pad of claim 17;
- o Pad D is an example of the fourth pad of claim 17;
- o Transmission gate 216a is an example of the second transmission gate of claim 17;

- o Output buffers 202b, 202c are examples of the first set of one or more other output buffers of claim 17;
- o Output buffers 202d, 202e, 202f are examples of the second set of one or more other output buffers of claim 17;
- o Transmission gates 214b, 214c are examples of the first set of one or more other transmission gates of claim 17;
- o Transmission gates 214d, 214e, 214f are examples of the second set of one or more other transmission gates of claim 17;
- o Transmission gates 216b, 216c are examples of the third set of one or more other transmission gates of claim 15; and
- o Transmission gates 216d, 216e, 216f are examples of the fourth set of one or more other transmission gates of claim 17.

McGowan does not teach or even suggest such a combination of features. As such, the Applicant submits that this provides additional reasons for the allowability of claim 17 over McGowan.

Claim 18

According to new claim 18, the first output buffer is a low-speed output buffer, and the PIC further comprises a high-speed output buffer adapted to present a second outgoing signal at the first pad. For at least some of the same reasons that original claim 12 is allowable, the Applicant submits that these reasons provide additional arguments for the allowability of claim 18 over McGowan.

Claim 19

According to new claim 19, the low-speed output buffer is a single-ended output buffer, and the high-speed output buffer is a double-ended output buffer. For at least some of the same reasons that original claim 13 is allowable, the Applicant submits that these same reasons provide additional arguments for the allowability of claim 19 over McGowan.

Claim 20

According to new claim 20, at least one single-ended output buffer is associated with at least two pads, wherein a transmission gate is connected between the at least one single-ended output buffer and each of its at least two associated pads.

McGowan does not teach or even suggest an output buffer connected to two different pads through two corresponding transmission gates. As such, the Applicant submits that this provides additional reasons for the allowability of claim 20 over McGowan.

Claim 21

According to new claim 21, the at least one double-ended output buffer and a first single-ended output buffer are both associated with a first pad.

McGowan does not teach or even suggest two different output buffer associated with a single pad, where one of the output buffers is a double-ended output buffer. As such, the Applicant submits that this provides additional reasons for the allowability of claim 21 (and therefore claims 22-23) over McGowan.

Claim 24

According to new claim 24, the programmable device further comprises a second pad, and the PIC further comprises a second transmission gate connected between the low-speed output buffer and the second pad. Thus, in the invention of new claim 24, the low-speed output buffer is connected (a) to the first pad through the first transmission gate and (b) to the second pad through the second transmission gate.

McGowan does not teach or even suggest an output buffer connected to two different pads through two corresponding transmission gates. As such, the Applicant submits that this provides additional reasons for the allowability of claim 24 over McGowan.

In view of the foregoing, the Applicant submits that the rejections of claims under 35 U.S.C. 102(b) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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